1. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said hard mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

2. The method according to claim 1 wherein said hard mask layer comprises silicon oxynitride.

3. The method according to claim 1 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

4. The method according to claim 1 wherein said step of stripping away said resist mask comprises a chemistry containing O_2 gas.

5. The method according to claim 1 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

6. The method according to claim 1 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He—O_2 gas, and combinations thereof.

7. The method according to claim 1 further comprising providing a silicon dioxide layer overlying said hard mask layer and underlying said resist layer.

8. The method according to claim 1 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etching chamber.

9. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

providing a hard mask layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said hard mask layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

10. The method according to claim 9 wherein said hard mask layer comprises silicon oxynitride.

11. The method according to claim 9 wherein said step of etching said resist mask to trim said resist mask comprises a chemistry containing O_2 gas.

12. The method according to claim 9 wherein said step of etching said hard mask layer comprises a chemistry of CF_4 gas.

13. The method according to claim 9 wherein said step of stripping away said resist layer comprises a chemistry containing O_2 gas.

14. The method according to claim 9 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

15. The method according to claim 9 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He—O_2 gas, and combinations thereof.

16. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a gate oxide layer overlying a semiconductor substrate;

providing a polysilicon layer overlying said gate oxide layer;

providing a silicon oxynitride layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said silicon oxynitride layer;

providing a resist layer overlying said silicon dioxide layer;

patterning said resist layer to form a resist mask that exposes a part of said silicon dioxide layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said silicon dioxide layer and said silicon oxynitride layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask wherein said etching comprises a main etch step followed by an overetch step; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

17. The method according to claim 16 wherein said step of etching said silicon dioxide layer and said silicon oxynitride layer comprises a chemistry of CF_4 gas.

18. The method according to claim 16 wherein said step of stripping away said resist layer comprises a chemistry containing O_2 gas.

19. The method according to claim 16 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He—O_2 gas, and combinations thereof.

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21. (Once Amended) A method of forming a semiconductor device, the method comprising:

providing a semiconductor substrate with a conductive layer formed thereon;

providing a hard mask layer above said conductive layer, said hard mask layer comprising silicon oxynitride;

providing a buffer layer above said hard mask layer;

providing a resist layer above said buffer layer;

patterning said resist layer to form a resist mask that exposes a part of said buffer layer; and

patterning said conductive layer in a dry plasma etch chamber, said patterning comprising:

etching said hard mask layer and said buffer layer exposed by said resist mask to form a hard mask that exposes a part of said conductive layer;

thereafter stripping away said resist mask; and

thereafter etching said conductive layer exposed by said hard mask.

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22. (Once Amended) The method of claim 21 wherein said buffer layer comprises an oxide.

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23. (Once Amended) The method of claim 21 wherein said buffer layer comprises silicon dioxide.

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24. (Once Amended) The method of claim 21 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

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28. (Once Amended) The method of claim 21 wherein said step of etching said conductive layer comprises a main etch step followed by an overetch step.

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26. (Once Amended) The method of claim 21 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etch chamber.

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27. (Once amended) A method for forming a semiconductor device, the method comprising:

providing a polysilicon layer overlying a semiconductor substrate;

providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer; and

patterning said polysilicon layer in a dry plasma etch chamber and wherein said patterning comprises:

etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

stripping away said resist mask in a first process step;

removing polymer residue resulting from said stripping step in a second process step; and

etching said polysilicon layer exposed by said hard mask.

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28. (New) The method of claim 27 wherein the step of patterning said polysilicon layer includes stripping away said hard mask.

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29. (New) The method of claim 27 further comprising cleaning away polymer residue from said hard mask after stripping away said resist mask.

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30. (New) The method of claim 27 wherein said hard mask layer comprises silicon oxynitride.

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31. (New) The method of claim 27 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

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32. (New) The method of claim 27 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

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33. (New) The method of claim 27 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etch chamber.

34 35. (Once Amended) The method of claim 33 wherein the steps of patterning said hard mask layer, removing said resist layer, and patterning said first layer are performed in a dry plasma etch chamber.

35 36. (Once Amended) The method of claim 33 wherein the step of patterning said hard mask layer includes etching the hard mask layer and the buffer layer.

36 37. (New) The method of claim 36 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

33 38. (Once Amended) A method for forming a semiconductor device, the method comprising:

providing a wafer having a substrate, a first layer formed on the substrate, a hard mask layer formed on the first layer, a buffer layer formed on said hard mask layer, and a resist layer formed on the buffer layer;

patterning said hard mask layer and said buffer layer to form a hard mask that exposes a part of said first layer;

removing said resist layer; and

patterning said first layer by etching said first layer and removing said hard mask layer and said buffer layer.

37 39. (New) The method of claim 33 wherein said step of etching said first layer comprises a main etch step followed by an overetch step.

38 40. (Once Amended) The method of claim 33 wherein the step of patterning said hard mask layer includes patterning a resist layer.

39 41. (New) The method of claim 40 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etch chamber.

40 42. (Once Amended) The method of claim 38 wherein said hard mask layer comprises silicon oxynitride.

41 43. (Once Amended) The method of claim 38 wherein said buffer layer comprises an oxide.

42 44. (Once Amended) The method of claim 38 wherein said buffer layer comprises silicon dioxide.

43 45. (Once amended) A method of forming a semiconductor device, the method comprising:

providing a semiconductor substrate with a conductive layer formed thereon;

providing a hard mask layer above said conductive layer;

providing a resist layer above said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer; and

patterning said conductive layer in a dry plasma etch chamber, said patterning comprising:

etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said conductive layer;

thereafter stripping away said resist mask using a first chemistry;

thereafter removing polymer residue using a second chemistry different from the first chemistry; and

thereafter etching said conductive layer exposed by said hard mask.

44 46. (New) The method of claim 45 wherein said hard mask layer comprises silicon oxynitride.

45 47. (New) The method of claim 45 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

46 48. (New) The method of claim 45 wherein said step of etching said conductive layer comprises a main etch step followed by an overetch step.

47 49. (New) The method of claim 45 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etch chamber.

49 51. (Once Amended) The method of claim 54 wherein the steps of patterning said hard mask layer, removing said resist layer, and patterning said first layer are performed in a dry plasma etch chamber.

50 52. (Once Amended) The method of claim 54 wherein the step of patterning said hard mask layer includes etching the hard mask layer.

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53. (New) The method of claim 52 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

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54. (Once Amended) A method for forming a semiconductor device, the method comprising:

providing a wafer having a substrate, a first layer formed on the substrate, a hard mask layer formed on the first layer, a buffer layer formed on said hard mask layer, and a resist layer formed on the buffer layer;

patterning said hard mask layer to form a hard mask that exposes a part of said first layer;

removing said resist layer; and

patterning said first layer by etching said first layer and removing said hard mask layer.

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55. (New) The method of claim 54 wherein said step of etching said first layer comprises a main etch step followed by an overetch step.

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56. (Once Amended) The method of claim 54 wherein the step of patterning said hard mask layer includes patterning a resist layer.

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57. (New) The method of claim 56 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etch chamber.

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58. (Once Amended) The method of claim 54 wherein said hard mask layer comprises silicon oxynitride.